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**DEVELOPMENT OF A Ge/GaAs HMT TECHNOLOGY  
BASED ON PLASMA-ENHANCED  
CHEMICAL VAPOR DEPOSITION**

**Quarterly Report -- Second Quarter**

**1 April, 1989 - 30 June, 1989**

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<p>The following report details the progress on ONR contract number N-00014-86-C-0838 during the period from April 1 to June 30, 1989. This program is targeted at development of a Ge on GaAs High Mobility Transistor (HMT) technology. During this quarter, the work has focused on 2 areas. The first area described involves the effect of the Si deposition parameters on the electrical characteristics of the composite Ge-pseudomorphic Si-SiO<sub>2</sub> MIS structure. Complementary n and p type Ge MIS structures are presented which exhibit low midgap D<sub>it</sub> values. The second area described involves the fabrication of Ge MISFET devices using the pseudomorphic Si-SiO<sub>2</sub> gate insulator. These n-channel transistors exhibit a transconductance of 24 mS/mm at a gate length of 2 microns.</p> <p style="text-align: right;">R.J. Markunas</p>					
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## 1.0 INTRODUCTION

The following report details the progress on ONR contract number N00014-86-C-0838 during the period from April 1 to June 30, 1989. Funding is being provided by the Strategic Defense Initiative under the Innovative Science and Technology division through the Office of Naval Research. This program is targeted at development of a Ge on GaAs High Mobility Transistor (HMT) technology.

During this quarter the work has focused on 2 primary areas. The first area described in section 2.0 involves the effect of the Si deposition parameters on the electrical characteristics of the composite Ge-pseudomorphic Si-SiO<sub>2</sub> MIS structure. There is a distinct correlation between deposition parameters which tend to yield the highest purity silicon and the interface state density of the device. Insights into chamber wall interactions with the process are discussed. Complementary n and p type Ge MIS structures are presented in section 2.1 which exhibit midgap  $D_{it}$  values of  $5 \times 10^{10} \text{cm}^{-2} \text{eV}^{-1}$ . The second area described in section 3.0 involves the fabrication of Ge MISFET devices using the pseudomorphic Si-SiO<sub>2</sub> gate insulator. These n-channel transistors exhibit a transconductance of 24 mS/mm at a gate length of 2 microns.

## 2.0 Ge MIS INTERFACIAL STUDIES - SILICON DEPOSITION PARAMETERS

The pseudomorphic Si interlayer is a crucial part of the Ge MIS technology being developed under this program. Optimization of the Si deposition process is thus an important part of the technology development. The first quarterly report

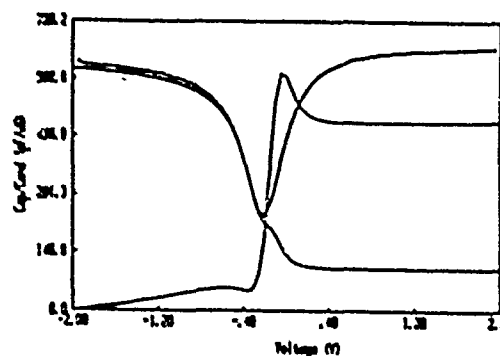
of this year described improvements which have been made in the Si deposition process by addition of hydrogen to the process gasses and by using low pressure conditions (60 to 70 mTorr). The hydrogen cuts the deposition rate in half and apparently increases the mobility of the depositing species on the surface. We have found that although the hydrogen can lead to better structural film properties, it can also lead to removal of contaminant species from the walls of the chamber (such as oxygen) which are subsequently incorporated into the films.

Figures 1 and 2 show capacitance voltage characterization of MIS structures with various Si deposition rates with and without hydrogen dilution. The structure characterized by Figure 1 had Si layers deposited at a rate of about 5 nm per minute with no hydrogen dilution and about 2.5 nm per minute with hydrogen dilution. In these cases the sample with the hydrogen dilution has a slightly lower  $D_{it}$  although neither structure exhibits any hysteresis in the high frequency characteristic. The structures characterized by Figure 2 had Si layers deposited at a rate of .5 nm per minute. In the case with hydrogen dilution there is hysteresis in the high frequency curve. The structure deposited with no hydrogen dilution at this rate has the lowest  $D_{it}$  of any Ge MIS structure to date. In this case, the hydrogen dilution has likely led to unintentional impurity incorporation (most likely oxygen) into the Si layer.

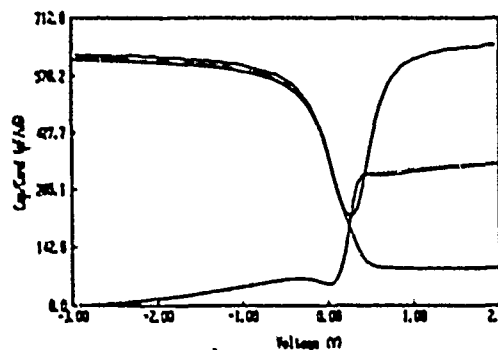
In both structure without hydrogen dilution, a slight bump is noted in the high frequency characteristics near the lower section of the curves. It is likely that this bump is caused by electron injection over the Ge-Si heterobarrier into the Si

# Ge MOS Interface Quality vs. Pseudomorphic Si Deposition Parameters

15 sec Si deposition  
no hydrogen dilution  
50 sccm silane



30 sec Si deposition  
with hydrogen dilution  
50 sccm silane



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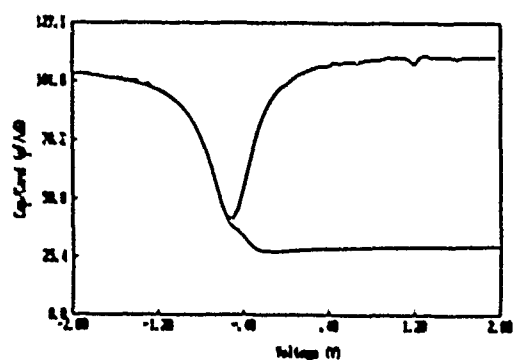
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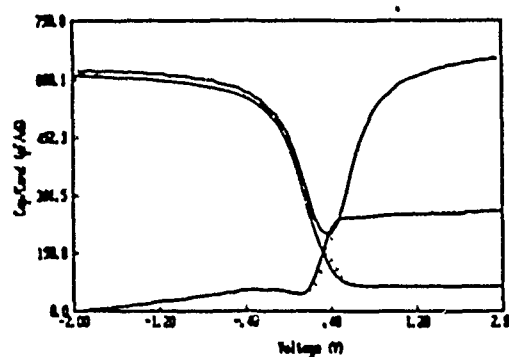
FIGURE 1 Capacitance voltage characteristics of Ge-Si-SiO<sub>2</sub> MIS structures with Si deposition rate of 5 nm/minute without hydrogen dilution and 2.5 nm/minute with hydrogen dilution.

## Ge MOS Interface Quality vs. Pseudomorphic Si Deposition Parameters

3 min Si deposition  
no hydrogen dilution  
5 sccm silane  
(smaller area capacitor)



3 min Si deposition  
with hydrogen dilution  
10 sccm silane



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- I RE 2 Capacitance voltage characteristics of Ge-Si-SiO<sub>2</sub> MIS structures with Si deposition rate of .5 nm/minute without hydrogen dilution and .5 nm/minute with hydrogen dilution.

layer. The metallurgical heterojunction is likely sharper without the hydrogen dilution. Thus the effect is somewhat washed out in the structures utilizing the hydrogen dilution. Note that the accumulation capacitance of these devices is lower than the inversion capacitance. It is probable that this effect is due to electron injection into the Si layer under inversion condition and blocking of hole injection under accumulation conditions. Thus the insulator is effectively thinner under inversion conditions. Although the Si is undoped, other depositions of Si on Si in the RPECVD system have always turned out n type. It may be possible to stop the electron injection by doping the Si layer p type.

## 2.1 Ge MIS Interfacial Studies - Complementary MIS

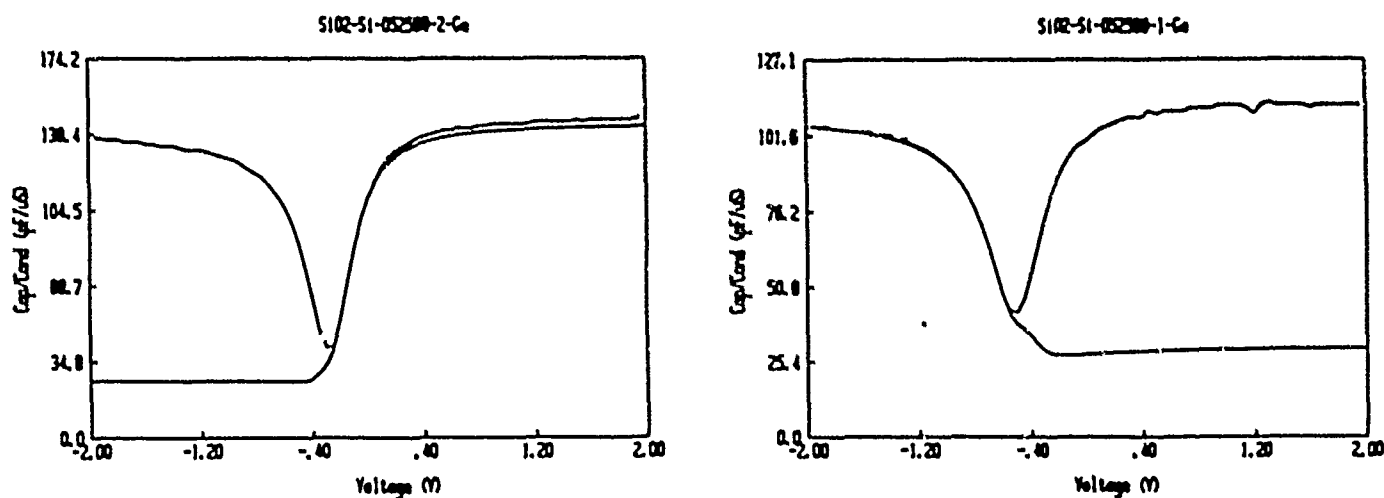
The pseudomorphic Si insulator technology has been applied successfully to both n and p type Ge material, illustrating that a complementary MIS technology is possible. The best complementary results to date are described in this section.

Figure 3 shows capacitance voltage data from both a p type and an n type Ge structure. The composite insulator structures used on these two samples were deposited identically. Both structures exhibit midgap  $D_{it}$  values of  $5 \times 10^{10} \text{cm}^{-2} \text{eV}^{-1}$ . There is no hysteresis in either high frequency characteristic.

Figure 4 shows a ramped current voltage breakdown characteristic for the composite insulator structure. The insulator thickness is about 15 nm. The insulator can sustain a field of about 9 to 10 MV/cm at a current level of 1 microamp.

## Complementary Ge MOS Structures

using the pseudomorphic Si/SiO<sub>2</sub> insulator



1 MHz and quasistatic capacitance voltage characteristics from n and p type Ge MOS capacitors. Interface State Densities at midgap are  $5 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ . The Si/SiO<sub>2</sub> insulator has a total thickness of approximately 15 nm.

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FIGURE 3 Capacitance voltage characteristics of n and p type Ge-Si-SiO<sub>2</sub> MIS structures.

SiO<sub>2</sub> Si 052589-1 Ge

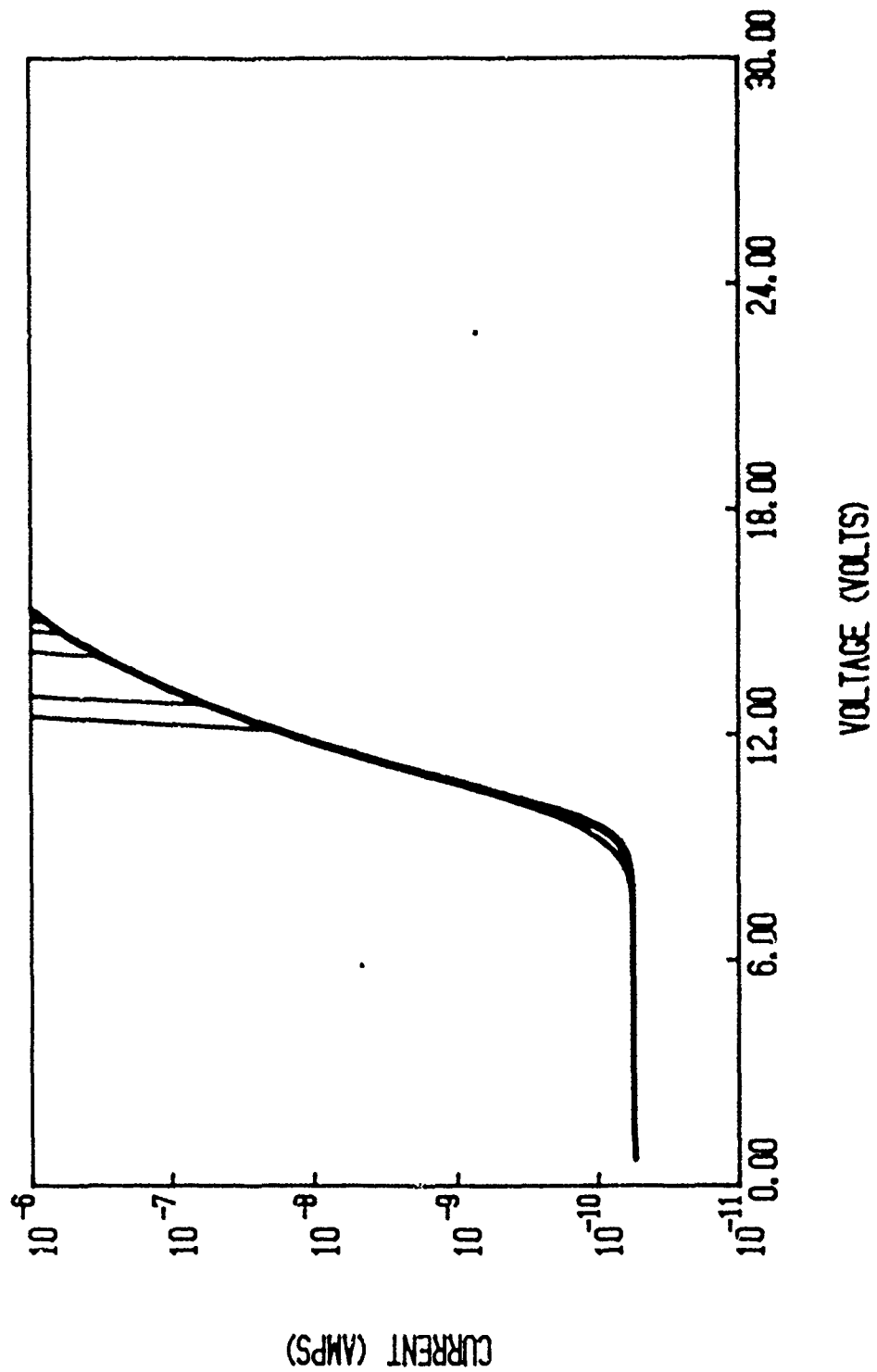


FIGURE 4 Current vs. ramped voltage characteristics of n and p type Ge-Si-SiO<sub>2</sub> MIS structures.

In both n and p type structures when electrons are attracted to the surface of the Ge, positive bias, the maximum quasistatic capacitance of the structure is somewhat higher than for the case where holes are attracted to the surface of the Ge. We take this as further evidence that electrons are being injected into the Si layer under positive bias conditions, and that holes are barred from injection by the energetics of the heterojunction. This phenomenon may in fact be very useful for the formation of a 2 dimensional carrier gas device by controlling the Si doping. A Ge MIS device with the carriers separated from the amorphous insulator interface by a crystalline layer could have near bulk carrier mobility.

### 3.0 Ge MISFET RESULTS

A mask set has been design and fabricated to allow fabrication of inversion mode MISFET devices. An illustration of this mask set is shown in Figure 5. The design includes on chip capacitors and a gated Hall pattern. The capacitors allow verification of interfacial characteristics of the gate insulator. The gated Hall pattern allows direct measurement of inversion carrier mobility and concentration.

The first set of working device has been fabricated. These devices are fabricated on a full 2 inch Ge wafer. The fabrication procedure is carried out as follows:

#### Ion Implantation Schedule

material-- Ge wafers p type (2 bare wafers)

implant species-- Phosphorus

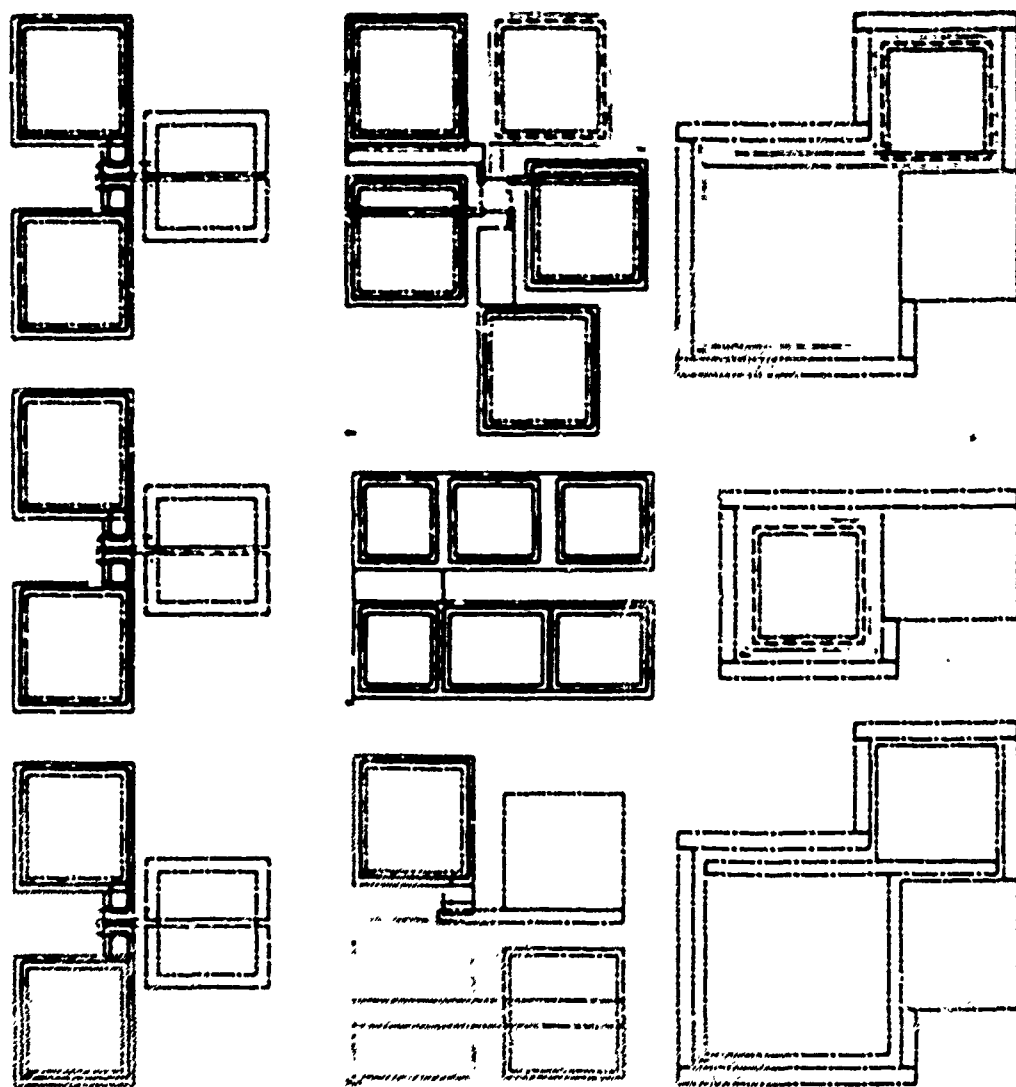


FIGURE 5: MISFET test die layout. MISFETs are on the extreme left arranged from top to bottom 2, 3, 4 micron gate lengths; gated Hall pattern is in the top center; contact resistance pad is in the center; DRAM storage cell is in the bottom center; capacitors are on the extreme right, top to bottom.

double implant dose-energy schedule

$1 \times 10^{14} \text{ cm}^{-2}$  at 100 KeV

$1 \times 10^{15} \text{ cm}^{-2}$  at 50 KeV

### Source Drain Formation

1. Solvent clean wafer in ultrasonic TCE, Acetone and Methanol.
2. Rinse wafer 5 minutes in running DI water.
3. Anneal the wafer at 500/(deC for 30 min in nitrogen.
4. Spin on photoresist at 4000 RPM.
5. Soft bake for 1 minute on hot plate at 90 °C.
6. Expose using 1 S/D (light field) mask.
7. Develop using 1 to 5 developer to water.
8. Rinse in water for 10 minutes. Blow dry, and HARD BAKE.
9. Etch wafer in Ge etching solution 1 minute (.27  $\mu\text{m}/\text{minute}$ ).

8:HPO<sub>4</sub> 48:H<sub>2</sub>O<sub>2</sub> 24: H<sub>2</sub>O

10. Rinse in water 5 min. then blow dry.

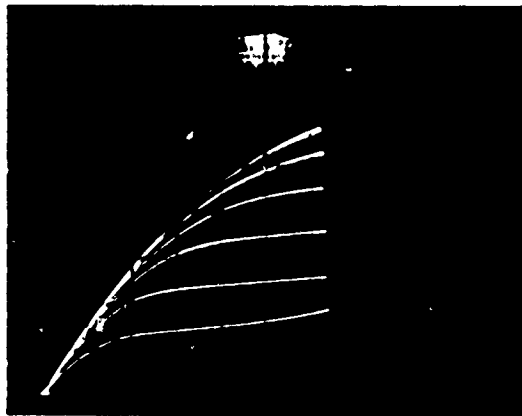
### Gate and Contact Formation

1. Deposit gate insulator structure on wafer.
2. Sputter deposit 15 min of Al on front side of wafer and 5 min on backside.
3. Anneal wafer 30 min at 400 °C.

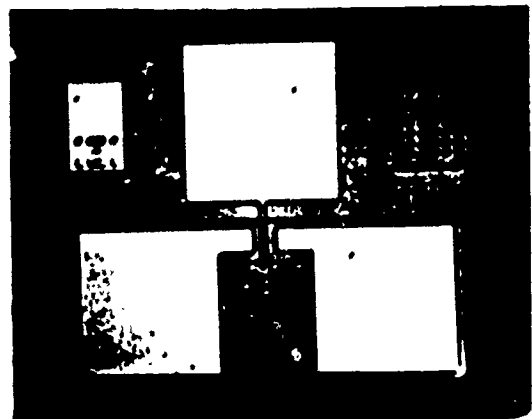
4. Spin on photoresist at 6000 rpm. Soft bake 1 min on 90 ° C hotplate.
5. Align and expose the wafer using 3 Gate (light field) mask.
6. Develop, rinse, blow dry and hard bake the wafer.
7. Etch the aluminum using Transene etchant A.
8. Remove photoresist with acetone, rinse in acetone, methanol, water, blow dry.
9. Dry wafer 1 minute on hot plate.
10. Spin on photoresist at 6000 rpm. Soft bake 1 min on 90 ° C hot plate.
11. Align and expose the wafer using 4 Contact (dark field) mask.
12. Develop, no hard bake. Etch 20 seconds in buffer HF, 1 min water rinse, blow dry.
13. Sputter deposit 5 min of Al on wafer.
14. Liftoff in acetone, rinse in fresh acetone, methanol, and water, blow dry.
15. Samples ready for testing.

The electrical characteristics of the devices are shown in Figures 6 and 7. Figure 6 shows the characteristic of a 4 micron gate length device. The maximum transconductance of this device is 20 mS/mm. Figure 7 shows the characteristic of a 2 micron gate length device. This device exhibits a maximum transconductance of 24 mS/mm. The fact that the transconductance does not scale with gate length indicates that the device has contact resistance problems. A larger problem is seen in the fact that the devices are not cut off at 0 volts. A check of the CV characteristics of the on chip capacitors (see Figure 8) indicated that the surface layer of

## Ge Enhancement Mode MOSFET



- 0.5 V/div
- 1.0 mA/div
- 1.0 V/step
- 1.0 mS/div
- 20 mS/mm
- max gain



- 4 micron gate length
- 50 micron gate width

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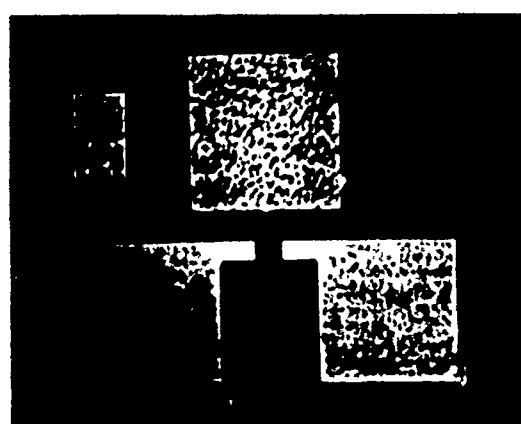
**FIGURE 6:** Drain characteristics of a 4 micron long by 50 micron wide Ge MISFET.

## Ge Enhancement Mode MOSFET



- 0.5 V/div
- 1.0 mA/div
- 1.0 V/step
- 1.0 mS/div

- 24 mS/mm  
max gain



- 2 micron gate  
length
- 50 micron gate  
width

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FIGURE 7: Drain characteristics of a 2 micron long by 50 micron wide Ge MISFET.

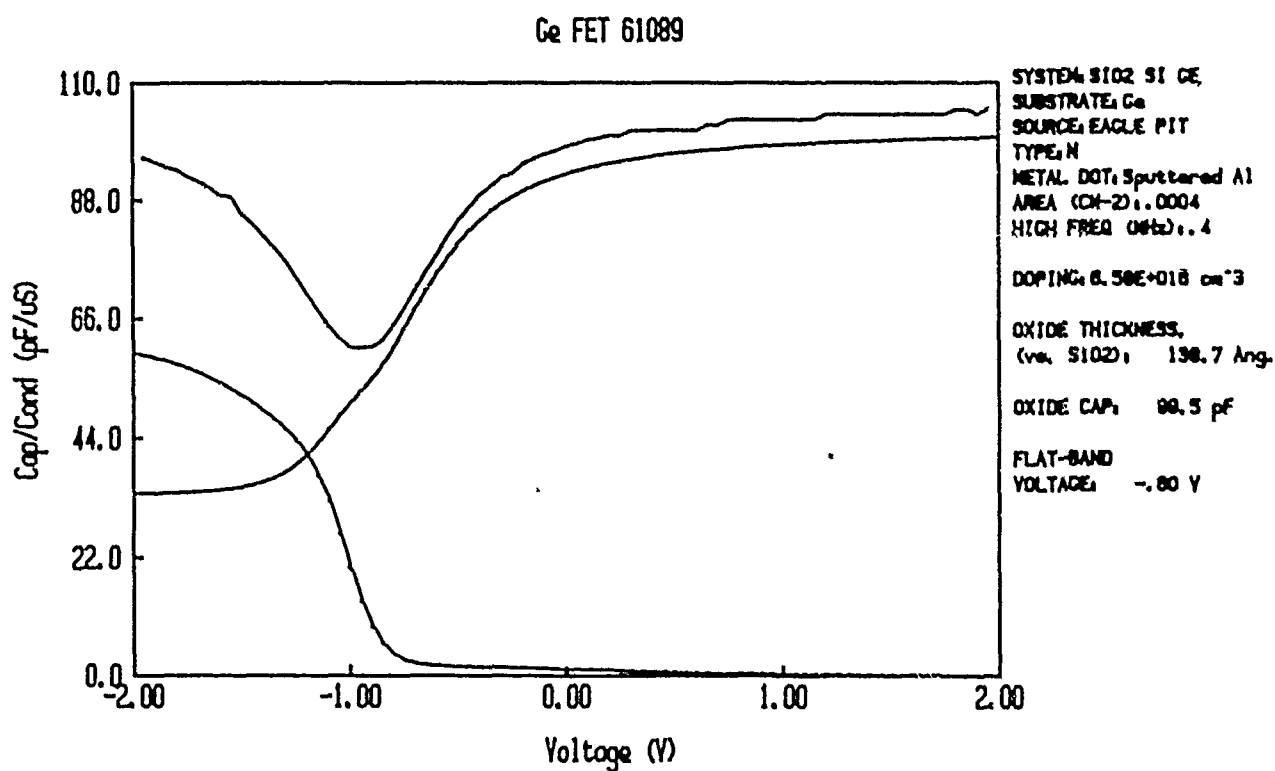


FIGURE 8: Capacitance voltage, conductance voltage characteristics of the MIS capacitors on chip with the MISFETS shown in Figures 6 and 7.

Ge material was n type instead of p type. It is likely that this was caused by under etching of the source drain mesa structures. In the future devices will be fabricated using selective source drain implants to avoid this problem.

#### 4.0 SUMMARY AND PREVIEW

During the quarter from April 1 to June 30 progress was made in the area of Ge insulator interface formation and in the area of Ge MISFET fabrication. MIS structures have been formed on both n and p type Ge with  $D_{it}$  values in the mid  $10^{10}\text{cm}^{-2}\text{eV}^{-1}$  range. Ge MISFET devices have been fabricated which exhibit transconductances of 24 mS/mm at a gate length of 2 microns.

During the next quarter work will continue on the Ge MISFET structures. The work will focus on selectively implanted n channel devices.